METHOD AND SYSTEM FOR MANAGING HARDWARE RESOURCES TO IMPLEMENT SYSTEM FUNCTIONS USING AN ADAPTIVE COMPUTING ARCHITECTURE

ABSTRACT OF THE DISCLOSURE

The present invention concerns a new category of integrated circuitry and a new methodology for adaptive or reconfigurable computing. The exemplary IC embodiment includes a plurality of heterogeneous computational elements coupled to an interconnection network. The plurality of heterogeneous computational elements include corresponding computational elements having fixed and differing architectures, such as fixed architectures for different functions such as memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability. In response to configuration information, the interconnection network is operative in real-time to configure and reconfigure the plurality of heterogeneous computational elements for a plurality of different functional modes, including linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, memory operations, and bit-level manipulations. The various fixed architectures are selected to comparatively minimize power consumption and increase performance of the adaptive computing integrated circuit, particularly suitable for mobile, hand-held or other battery-powered computing applications. In an exemplary embodiment, some or all of the computational elements are alternately configured to implement two or more functions.